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EXAMINER	
PARK, ILWOO	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 08/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/630,635	ROONEY, JEFFREY JAY	
	Examiner	Art Unit	
	Ilwoo Park	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 2, 10, 17, 31, and 37 are amended in response to the last office action. The following rejections now apply. Bennett, Coke, and Lange were cited in the last office action. Claims 2-42 are presented for examination.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 8, 13, 18, 30, 36, and 38 contain the trademark/trade name "Intel Pentium®". Where a trademark or trade name is used in a claim as a limitation to identify or describe a particular material or product, the claim does not comply with the requirements of 35 U.S.C. 112, second paragraph. See *Ex parte Simpson*, 218 USPQ 1020 (Bd. App. 1982). The claim scope is uncertain since the trademark or trade name cannot be used properly to identify any particular material or product. A trademark or trade name is used to identify a source of goods, and not the goods themselves. Thus, a trademark or trade name does not identify or describe the goods associated with the trademark or trade name. In the present case, the trademark/trade name is used to identify/describe processors and, accordingly, the identification/description is indefinite.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 2-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Bennett, US patent No. 5,426,740.

As to claim 2, Bennett teaches a method for providing data transfers between a processor [CPU module 12] and a component [I/O controller 16], the method comprising:

buffering [col. 7, lines 14-17] an address with a first buffer, the first buffer being in communication with a processor and a component, wherein the processor operates at a different speed [col. 2, lines 28-43] than the component;

buffering [col. 7, lines 14-17] a data value with a second buffer, the second buffer being in communication with the processor and the component;

controlling [integrated I/O bus interface controller 122 in fig. 7; col. 6, lines 30-46] the first buffer and the second buffer as a matched pair [set of bi-directional address and data buffers 82] such that the address held in the first buffer corresponds to the data value held in the second buffer; and

controlling bi-directional data flow [fig. 7] through the second buffer such that data flows between the processor and the component .

6. As to claim 3, Bennett teaches the first and second buffers are in communication with the processor via a bus [fig. 7].

7. Claims 2-3, 10, 17, and 37 are rejected under 35 U.S.C. 102(b) as being anticipated by Coke, US patent No. 5,455,915.

As to claim 2, Coke teaches a method for providing data transfers between a processor [CPU 11 in fig. 1] and a component [secondary bus devices in fig. 1], the method comprising:

buffering an address with a first buffer [LB 33a, PWB 37a in fig. 2], the first buffer being in communication with a processor and a component, wherein the processor operates at a different speed [col. 1, lines 30-45] than the component;

buffering ~~a data value with a second~~ buffer [LB 33d, PWB 37d in fig. 3], ~~the~~ second buffer being in communication with the processor and the component;

controlling [col. 5, lines 10-20] the first buffer and the second buffer as a matched pair such that the address held in the first buffer corresponds to the data value held in the second buffer; and

controlling bi-directional data flow [from bus 12 to bus 18 via 35d, 38d, 33d, 43d, and 41d for one direction and from bus 18 to bus 12 via 36d, 39d, 33d, 43d, 49d, and 40d for other direction] through the second buffer such that data flows between the processor and the component.

8. As to claim 3, Coke teaches the first and second buffers are in communication with the processor via a bus [fig. 1].

9. As to claim 10, Coke teaches a method for controlling data transfers between a processor [CPU 11 in fig. 1] and a component [secondary bus devices in fig. 1], the method comprising:

buffering with a plurality of address buffers [LB 33a, PWB 37a in fig. 2] address requests from a processor to a component, wherein the processor operates at a different speed [col. 1, lines 30-45] than the component;

bi-directionally buffering [from bus 12 to bus 18 via 35d, 38d, 33d, 43d, and 41d for one direction and from bus 18 to bus 12 via 36d, 39d, 33d, 43d, 49d, and 40d for other direction] with a plurality of data buffers [LB 33d, PWB 37d in fig. 3] data transfers between the processor and the component; and

controlling [col. 5, lines 10-20] said buffering address requests and said bi-directionally buffering such that each of the buffered data transfers relates to an address held in one of the plurality of address buffers.

10. As to claim 17, Coke teaches a method for providing data transfers between a processor [CPU 11 in fig. 1] and a component [secondary bus devices in fig. 1], the method comprising:

buffering a first address buffer [LB 33a, PWB 37a in fig. 2] with a first address;

buffering a second address buffer [LB 33a, PWB 37a in fig. 2] with a second address;

buffering a first data buffer [LB 33d, PWB 37d in fig. 3] with a first data value;

buffering a second data buffer [LB 33d, PWB 37d in fig. 3] with a second data value;

controlling [col. 5, lines 10-20] the first address buffer and the first data buffer as a matched pair such that the first address corresponds to the first data value; and

controlling bi-directional data flow [from bus 12 to bus 18 via 35d, 38d, 33d, 43d, and 41d for one direction and from bus 18 to bus 12 via 36d, 39d, 33d, 43d, 49d, and 40d for other direction] through the first data buffer such that data flows between a processor and a component, wherein the first and second address buffers and the first and second data buffers are each in communication with the processor and the component, and wherein the processor operates at a different speed [col. 1, lines 30-45] than the component.

11. As to claim 37, Coke teaches an apparatus for controlling data transfers between a processor [CPU 11 in fig. 1] and a component [secondary bus devices in fig. 1], the apparatus comprising:

means [LB 33a, PWB 37a in fig. 2] for buffering address requests from a processor to a component, wherein the processor operates at a different speed [col. 1, lines 30-45] than the component;

means [LB 33d, PWB 37d in fig. 3] for bi-directionally buffering [from bus 12 to bus 18 via 35d, 38d, 33d, 43d, and 41d for one direction and from bus 18 to bus 12 via 36d, 39d, 33d, 43d, 49d, and 40d for other direction] data transfers between the processor and the component; and

control logic [col. 5, lines 10-20] for controlling the means for buffering and the means for bi-directionally buffering so that each of the buffered data transfers relates to an address held in the means for buffering.

12. Claims 2-21 and 37-42 are rejected under 35 U.S.C. 102(e) as being anticipated by Lange, US patent No. 5,978,878.

As to claim 2, Lange teaches a method for providing data transfers between a processor [CPU in col. 2, lines 61-67] and a component [peripheral devices in col. 2, lines 61-67], the method comprising:

buffering [PCI buffers 90, 98 in fig. 2B] an address with a first buffer, the first buffer being in communication with a processor and a component, wherein the processor operates at a different speed [col. 1, lines 20-28; col. 3, line 1] than the component;

buffering [PCI buffers 90, 98] a data value with a second buffer, the second buffer being in communication with the processor and the component;

controlling [fig. 4] the first buffer and the second buffer as a matched pair [address/data buffers: col. 5, lines 51-55] such that the address held in the first buffer corresponds to the data value held in the second buffer; and

controlling bi-directional data flow [fig. 7; col. 5, line 65-col. 6, line 1] through the second buffer such that data flows between the processor and the component .

13. As to claim 3, Lange teaches the first and second buffers are in communication with the processor via a bus [fig. 1].

14. As to claim 4, Lange teaches the first and second buffers are in communication with the bus via a bus master controller and a bus slave controller [fig. 2B].

15. As to claim 5, Lange teaches the first buffer further comprises status bits [e.g., type(4) in PCI buffers 90, 98].

16. As to claim 6, Lange teaches the status bits relate to the type of request being made by the processor [e.g., type(4) in PCI buffers 90, 98].

17. As to claim 7, Lange teaches said act of controlling the first buffer and the second buffer as a matched pair is performed with pointers [col. 6, lines 30-46].

18. As to claims 8, 13, 18, and 38, Lange teaches the processor is from an Intel Pentium® family of processors [col. 2, line 67-col. 3, line 3].

19. As to claims 9 and 21, Lange teaches the said act of controlling bi-directional data flow is performed with at least one input data arbiter [primary and secondary PCI interfaces: fig. 4].

20. As to claim 10, Lange teaches a method for controlling data transfers between a processor [CPU in col. 2, lines 61-67] and a component [peripheral devices in col. 2, lines 61-67], the method comprising:

buffering [PCI buffers 90, 98 in fig. 2B] with a plurality of address buffers address requests from a processor to a component, wherein the processor operates at a different speed [col. 1, lines 20-28; col. 3, line 1] than the component;

bi-directionally buffering [PCI buffers 90, 98 in fig. 2B] with a plurality of data buffers data transfers between the processor and the component; and

controlling [integrated I/O bus interface controller 122 in fig. 7; col. 6, lines 30-46] said buffering address requests and said bi-directionally buffering such that each of the buffered data transfers relates to an address held in one of the plurality of address buffers.

21. As to claim 11, Lange teaches additionally comprising indicating which of the plurality of data buffers is available to accept new data [col. 7, lines 54-65].

22. As to claim 12, Lange teaches said act of indicating is performed with reference pointers [col. 6, lines 30-46].

23. As to claim 14, Lange teaches said act of buffering address requests includes the use of an input arbiter and an output arbiter [primary and secondary PCI interfaces].

24. As to claim 15, Lange teaches said act of bi-directionally buffering is performed with an input arbiter and an output arbiter [primary and secondary PCI interfaces].

25. As to claim 16, Lange teaches the plurality of address buffers comprises at least three address buffers and wherein the plurality of data buffers comprises at least three data buffers [col. 7, lines 54-65].

26. As to claim 17, Lange teaches a method for providing data transfers between a processor [CPU in col. 2, lines 61-67] and a component [peripheral devices in col. 2, lines 61-67], the method comprising:

buffering [col. 5, lines 51-55] a first address buffer [PCI buffers 90, 98 in fig. 2B] with a first address;

buffering [col. 5, lines 51-55] a second address buffer [PCI buffers 90, 98 in fig. 2B] with a second address;

buffering [col. 5, lines 51-55] a first data buffer [PCI buffers 90, 98 in fig. 2B] with a first data value;

buffering [col. 5, lines 51-55] a second data buffer [PCI buffers 90, 98 in fig. 2B] with a second data value;

controlling the first address buffer and the first data buffer as a matched pair [address/data buffers: col. 5, lines 51-55; fig. 6] such that the first address corresponds to the first data value; and

controlling bi-directional data flow [fig. 7; col. 5, line 65-col. 6, line 1] through the first data buffer such that data flows between a processor and a component, wherein the first and second address buffers and the first and second data buffers are each in communication with the processor and the component, and wherein the processor operates at a different speed [col. 1, lines 20-28; col. 3, line 1] than the component.

27. As to claim 19, Lange teaches the first and second address buffers and the first and second data buffers are in communication with the processor via a bus [fig. 1].

28. As to claim 20, Lange teaches said act of controlling the first address buffer and the first data buffer as a matched pair is performed with pointers [col. 6, lines 30-46].

29. As to claim 37, Lange teaches an apparatus for controlling data transfers between a processor [CPU in col. 2, lines 61-67] and a component [peripheral devices in col. 2, lines 61-67], the apparatus comprising:

means [PCI buffers 90, 98 in fig. 2B; col. 5, lines 51-55] for buffering address requests from a processor to a component, wherein the processor operates at a different speed [col. 1, lines 20-28; col. 3, line 1] than the component;

means [PCI buffers 90, 98 in fig. 2B; col. 5, lines 51-55] for bi-directionally buffering data transfers between the processor and the component; and

control logic [integrated I/O bus interface controller 122 in fig. 7; col. 6, lines 30-46] for controlling the means for buffering and the means for bi-directionally buffering so

that each of the buffered data transfers relates to an address held in the means for buffering.

30. As to claim 39, Lange teaches means for buffering includes a plurality of address buffers [col. 7, lines 54-65].

31. As to claim 40, Lange teaches means for bi-directionally buffering includes a plurality of data buffers [col. 7, lines 54-65].

32. As to claim 41, Lange teaches means for buffering includes an input arbiter and an output arbiter [primary and secondary PCI interfaces].

33. As to claim 42, Lange teaches means for bi-directionally buffering includes an input arbiter and an output arbiter [primary and secondary PCI interfaces].

Claim Rejections - 35 USC § 103

34. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

35. Claims 23 and 25-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rabe et al., US patent No. 5,664,122 in view of Bennett, US patent No. 5,426,740.

As to claim 23, Rabe et al teach a method for transferring addresses and data through a buffer, the method comprising:

storing an address in a first buffer [e.g., register 44 in fig. 4] in communication with a first component and a second component, the first buffer including status bits [e.g., four bit registers 42, 43: col. 7, lines 30-40];

storing data in a second buffer [e.g., buffers 31, 32 in fig. 4] matched with said first buffer so that the address stored in the first buffer is related to the data stored in the second buffer; and

providing signals with an arbiter [col. 7, lines 40-44; col. 9, lines 28-35] in communication with said status bits so as to grant access to the first buffer and to the second buffer such that a second address can be written to the first buffer while [col. 8, lines 56-64; col. 9, lines 43-51] data is read from the second buffer.

However, Rabe et al do not explicitly disclose the buffer is a bi-directional buffer. Bennett teaches a method for transferring addresses and data through a bi-directional buffer [bidirectional address/data buffers 62 in fig. 7] between components. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the buffer being a bi-directional buffer in order to increase efficiency in the transfer between components [Bennett: col. 7, lines 14-17].

36. As to claim 25, Rabe et al teach the status bits comprise transfer type bits indicative of the status of a data transfer from the first component to the second buffer [col. 7, lines 30-40].

37. As to claim 26, Rabe et al teach the first component comprises a memory [col. 1, lines 57-60].

38. As to claim 27, Rabe et al teach the first component comprises a processor [col. 1, lines 57-60].

39. As to claim 28, Rabe et al teach the first buffer is in communication with the processor via a bus [col. 1, lines 57-60].

40. As to claim 29, Rabe et al teach the first buffer is in communication with the bus via a bus master controller and a bus slave controller[col. 4, lines 15-23].

41. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bennett and Rabe et al as applied to claim 23 above, and further in view of Lange, US patent No. 5,978,878.

As to claim 24, Bennett and Rabe et al do not explicitly teach the status bits comprise transfer type bits indicative of the status of an address transfer from the first component to the second buffer. Lange teaches the status bits comprise transfer type bits [type(4) in PCI buffers 90, 98 in fig. 2B] indicative of the status of an address transfer from the first component to the second buffer. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made the status bits to include transfer type bits indicative of the status of an address transfer from the first component to the second buffer in order to increase flexibility in control of PCI bus transactions [Lange: col. 5, lines 5-22].

42. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bennett and Rabe et al as applied to claim 27 above, and further in view of Lange, US patent No. 5,978,878.

As to claim 30, Bennett and Rabe et al teach the processor is from Intel family of processors [Rabe et al: col. 3, lines 53-53]. However, Bennett and Rabe et al do not teach the Intel family of processors includes Intel Pentium family of processors. Lange teaches a method for transferring data between a processor and a component and the processor is from Intel Pentium family of processors. Therefore, it would have been

obvious to one of ordinary skill in the art at the time the invention was made to include a processor from Intel Pentium family of processors in order to increase processing speed and power.

43. Claims 31-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rice, US patent No. 6,195,721 in view of Rabe et al., US patent No. 5,664,122.

As to claim 31, Rice teaches a method for transferring data between a processor [e.g., processor #1 in fig. 1] and a component [e.g., processor #2 in fig. 1] utilizing a plurality of address buffers and a plurality of data buffers [col. 4, lines 25-29], the method comprising:

receiving [col. 2, lines 13-15] a data request including an associated address from a processor;

storing [col. 2, lines 15-20] the associated address in a first address buffer;

transmitting [col. 2, lines 28-33] with a first bi-directional data buffer associated with the first address buffer a data request including said associated address to a component; and

receiving [col. 2, lines 33-36] data from the component in the first bi-directional data buffer.

Though Rice teaches a method controlling an address buffer and an associated data buffer for storing address and data between two buses having different bus speeds [col. 2, line 66-col. 3, line7] each other, Rice does not expressly disclose determining whether the buffers are available. Rabe et al teach a method controlling an address buffer [e.g., register 44 in fig. 4] and an associated data buffer [e.g., data buffers 31,32

in fig. 4] for storing address and data between two buses having different bus speeds [abstract] each other and further teach determining whether an address buffer and an associated data buffer are available [col. 7, lines 40-44; col. 9, lines 28-35]. Therefore, it would have been obvious to one of ordinary skill in the art of a buffer control at the time the invention was made to combine the two teachings of Rice and Rabe et al because they both teach controlling and using buffers for storing address and data to alleviate the difference of bus speeds and the Rabe et al's teaching of determining whether an address buffer and an associated data buffer are available would increase reliability by ~~preventing overwrite or data loss [Rabe et al~~: col. 7, lines40-44; col. 10, lines 10-13] of communication between the two buses of Rice.

44. As to claim 32, Rabe et al teach receiving the address into the first address buffer while data is being read from the first data buffer [col. 8, lines 56-64].

45. As to claim 33, Rice teaches the first address buffer and the first data buffer are in communication with the processor via a bus [fig. 1].

46. As to claim 34, Rabe et al teach the first address buffer and the first data buffer are in communication with a bus via a bus master controller and a bus slave controller [fig. 1].

47. As to claim 35, Rice teaches the first address buffer and the first data buffer are associated with each other through the use of pointers [col. 2, lines 3-126].

48. Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rice and Rabe et al as applied to claim 31 above, and further in view of Lange, US patent No. 5,978,878.

As to claim 36, Rice and Rabe et al teach the processor is from Intel family of processors [Rabe et al: col. 3, lines 53-53]. However, Rice and Rabe et al do not teach the Intel family of processors includes Intel Pentium family of processors. Lange teaches a method for transferring data between a processor and a component and the processor is from Intel Pentium family of processors. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a processor from Intel Pentium family of processors in order to increase processing speed and power.

49. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lange, US patent No. 5,978,878 in view of Rabe et al., US patent No. 5,664,122.

As to claim 22, Lange teaches controlling the first address buffer and the first data buffer as a matched pair. However, Lange does not explicitly disclose the buffer control allowing data to be read from the first data buffer while an address is written to the first address buffer. Rabe et al teach a method for providing data transfers between a processor and a component controlling a first address buffer and a first data buffer and the buffer control allowing data to be read from a first data buffer while [col. 8, lines 56-64; col. 9, lines 43-51] an address is written to a first address buffer. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the buffer control allowing data to be read from a first data buffer while an address is written to a first address buffer in order to increase efficiency in the buffer control of Lange having multiplexed address and data.

Conclusion

50. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ilwoo Park whose telephone number is (571) 272-4155. The examiner can normally be reached on Monday through Friday from 9:00 AM to 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dov Popovici can be reached on (571) 272-4083. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ILWOO PARK
PRIMARY EXAMINER

Ilwoo Park
August 09, 2005